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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,336	05/30/2001	Lucas P. Curtis	81837DMW	7712

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EXAMINER	
YE, LIN	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 09/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,336	CURTIS ET AL.	
	Examiner	Art Unit	
	Lin Ye	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/30/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1-2, 4-6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Charneski et al. U.S. Patent 5,982,428.

Referring to claim 1, the Charneski reference discloses in Figures 4 and 5, a clock synthesizing circuit (master clocks 19 and CCD clock generator 12, see Col. 2, lines 46-60) for generating a plurality of lower frequency (pixel clock PIXE_CLK) clock signals (20) from a higher frequency clock (nX pixel clock PIXE_CLK_nX, n can be 4, 6, 8 or any integer number great than 1) for driving a pixel-based image sensor, said synthesizing circuit comprising: a pixel rate generator (master clocks 19) that generates a master clock having a master clock frequency (equal to PIXEL_CLK frequency) corresponding generally to a readout rate of the image sensor; a frequency locked loop (phase locked loop 72 in the CCD Clock generator 12) that receives the master clock (PIXEL_CLK) and generates a high frequency clock (PIX_CLK_nX) operating at a multiple (n can be 4, 6, 8 or any integer number great than 1) of the master clock frequency; and a clock generation circuit (CCD Clock generator 12 includes a Modulo MUX 78 and phase MUX 76) that utilizes the high

frequency clock to generate a plurality of low frequency clock signals (to the output 1-8) for driving the image sensor (See Col. 37-63).

Referring to claim 2, the Charneski reference discloses the frequency locked loop (72) is a phase locked loop in Figure 4.

Referring to claim 4, the Charneski reference discloses wherein the clock generation circuit (12) utilizes the edge transitions of the high frequency clock to generate the plurality of low frequency clock signals for driving the image sensor (See Col. 4, lines 37-45).

Referring to claim 5, the Charneski reference discloses wherein the clock generation circuit (12) generates a high frequency shift register (74) clock for reading out the image sensor (one of output clock signals 20 for reading out the image sensor to the analog signal processing).

Referring to claim 6, the Charneski reference discloses wherein the clock generation circuit generates a high frequency reset clock for the image sensor (See Col. 3, lines 66-67 and Col. 4, lines 1-2).

Referring to claim 8, the Charneski reference discloses wherein the clock generation circuit further generates one or more further low frequency clock signals (the clock signals 20 are relatively low frequency PIXEL_CLK) for driving electronics associated with the image sensor (See Col. 2, lines 51-60).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Charneski et al. U.S. Patent 5,982,428 in view of Sidiropoulos et al. IEEE Vol. 32, NO. 11, November 1997, "A Semidigital Dual Delay-Locked Loop" (hereinafter referred as Sidiropoulos).

Referring to claim 3, the Charneski reference discloses all subject matter as discussed in respected claim 1, except that the reference does not explicitly show the frequency locked loop also is a delay locked loop instead of phase locked loop.

The Sidiropoulos reference discloses a clock system can either use both phase-looked loops and delay-locked loops for increasing clock speeds without undesirable levels of radiated electromagnetic interference (See page 1683, Introduction). The Sidiropoulos reference is evidence that one of ordinary skill in the art at the time to see more advantages for a clock synthesizing circuit has a flexible option to use either both phase-looked loops and delay-locked loops for increasing clock speeds so that the loop achieves large operating range and low jitter. For that reason, it would have been obvious to see the frequency locked loop also is a delay locked loop disclosed by Charneski.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Charneski et al. U.S. Patent 5,982,428 in view of Tao U.S. 6,285,399.

Referring to claim 7, the Charneski reference discloses all subject matter as discussed in respected claim 1, except that the reference does not explicitly show the clock generation

(12) circuit includes a counter and one or more comparators pairs whose outputs are logically combined to form one or more pixel rate clocks.

The Tao reference discloses in Figures 7-9, the clock generation circuit (Timing ASIC 226) includes a counter (the pixel counter 830 in Figure 8) driven by the master clock (OSC 716 in Figure 7) that feeds one or more comparator pairs (comparator 834 in horizontal timing generator 728 and comparator 934 in Vertical timing generator 736) whose outputs are logically combined to form one or more pixel rate clocks (horizontal outputs 854 and Vertical outputs 954) (Col. 5, lines 45-56). The Tao reference is evidence that one of ordinary skill in the art at the time to see more advantages for a clock generation circuit can use of various other configurations of hardware and/or software devices such as counter and comparators so that a image device is thus able to more efficiently and effectively capture image data. For that reason, it would have been obvious to see the clock generation (12) circuit includes a counter and one or more comparators pairs whose outputs are logically combined to form one or more pixel rate clocks with programmable rising and falling edge positions disclosed by Charneski.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Charneski et al. U.S. Patent 5,982,428 in view of Petilli European Publication EP 0793381 A2.

Referring to claim 9, the Charneski reference discloses all subject matter as discussed in respected claim 8, except that the reference does not explicitly show the clock generation (12) circuit generates high frequency clamp and sample clocks for a correlated double sampling circuit.

The Petilli reference discloses in Figures s 3 and 4, a clock generation circuit (35) generates high frequency (i.e. 4 times clock pixel clock rate) clamp and sample clocks for a correlated double sampling circuit (CDS) (See Col. 4, lines 53-59 and Col. 5, lines 1-15). The Petilli reference is evidence that one of ordinary skill in the art at the time to see more advantages for a clock generation circuit supplies the clock signals to the CDS and the image sensor CCD so that the clock generation circuit, CDS and CCD can be built in a single chip and significantly reducing the package cost (See Col. 3, lines 1-5). For that reason, it would have been obvious to see the clock generation (12) circuit generates high frequency clamp and sample clocks for a correlated double sampling circuit disclosed by Charneski.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Charneski et al. U.S. Patent 5,982,428 in view of Jacobs U.S. Patent 6,580,456.

Referring to claim 10, the Charneski reference discloses all subject matter as discussed in respected claim 8, except that the reference does not explicitly show the clock generation (12) circuit generates high frequency clock for an analog to digital converter circuit (A/D).

The Jacobs reference discloses in Figure 2, the clock generation circuit (programmable timing generator 204) generates clock signals for DSP (206), ASP (211) and A/D Convert (212) (See Col. 3, lines 42-54). The Jacobs reference is evidence that one of ordinary skill in the art at the time to see more advantages for a clock generation circuit supplies the clock signals to the image sensor, ASP, A/D and DSP so that the digital image data between the ASP, the A/D and DSP can be synchronize efficiently. For that reason, it would have been obvious to see the clock generation (12) circuit generates high frequency clock (e.g., as

discussed in claim 1, the frequency locked loop has adjust clocks signal to a relatively high frequency, such 4 times or more clock pixel clock rate) for an analog to digital converter circuit (A/D) disclosed by Charneski.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

   a. MacLean U.S 5,144,444 discloses a method for improving the output response of electronic imaging system.

   b. Kubo et al. U.S. 6,680,751 discloses a timing pulse generating apparatus generates a variety of timing pulses used for acquiring image signals.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Lin Ye** whose telephone number is **(703) 305-3250**. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on (703) 308-9644.

   Any response to this action should be mailed to:

   Commissioner of Patents and Trademarks

   Washington, DC. 20231

   Or faxed to:

   (703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Lin Ye
September 3, 2004

ANDREW CHRISTENSEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600